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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/815,201	03/31/2004	Jhon Jhy Liaw	N1280-00180(TSMC2003-1083	9501

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EXAMINER	
FENTY, JESSE A	

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 04/20/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/815,201	LIAW, JHON JHY	
	Examiner	Art Unit	
	Jesse A. Fenty	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 February 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 and 3-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 and 3-25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

Claim 24 is objected to because of the following informalities: Claim 24 appears to contain a typographical error in line 1. The words "further" and "wherein" are both used instead of one in the alternative to further limit the claim. Appropriate correction is required.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1 and 3-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Noda (U.S. Patent No. 6,512,299 B1) in view of Bryant et al. (U.S. Patent No. 6,436,744 B1).

In re claim 1, Noda (e.g., Figs. 3-4) discloses a semiconductor contact connection structure comprising:

a substrate (11/51);

a first semiconductor device formed on the substrate;

a non-conducting gate interconnect layer formed on the substrate for connecting to a gate of a second semiconductor device formed on the insulator substrate; and

a silicide layer (23) formed on the gate interconnect layer, and an active region of the first semiconductor device for making a connection thereof, wherein the silicide layer is a sidewall butted connection structure that bridges a dielectric edge portion (13) separating the gate interconnect structure from the active region and the silicide layer is a continuous layer including a junction covering the dielectric edge portion and consisting of a first silicide film formed of silicon from the gate interconnect layer and a second silicide film formed of silicon from the active region (described in column 5, lines 66-67 through column 6, lines 1-4).

Noda does not expressly disclose an insulating substrate for this buried contact structure. Bryant discloses the use of an SOI substrate for buried contact devices. It would have been obvious for one skilled in the art at the time of the invention to use an SOI substrate as disclosed by Bryant for the buried contact structure of Noda for the purpose, for example, of enhancing the device structure by avoiding floating body effects (Bryant; column 2, lines 51-53).

In re claim 3, Noda in view of Bryant disclose the device of claim 1, wherein the silicide layer further covers a sidewall of the gate interconnect.

In re claim 4, Noda in view of Bryant disclose the device of claim 1, wherein the first semiconductor device is formed on a silicon based material on the insulator substrate wherein the silicon based material has a thickness of more than 20 angstroms (Bryant; column 5, lines 25-26).

In re claim 5, Noda in view of Bryant disclose the device of claim 1, wherein the active region serves as a local connection layer between the first and second semiconductor devices.

In re claim 6, Noda in view of Bryant disclose the device of claim 1, wherein the silicide layer is less than 350 angstroms in thickness (Noda; column 5, lines 64-65 discloses a thickness of 30 nm, which equates to 300 angstroms).

In re claim 7, Noda in view of Bryant disclose the device of claim 1, wherein the silicide layer provides an electrical resistance of 100 ohm/ea, or less (based on the thickness of the layer), between the gate interconnect layer and the active region.

Claims 8-25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Noda in view of Bryant and further in view of Sundaresan (U.S. Patent No. 5,298,782).

In re claims 8 and 15, Noda in view of Bryant discloses an SRAM cell formed on an insulator substrate, the cell comprising:

at least one active region with a continuous silicide layer (23) formed thereon serving as an intra-cell connection layer connection drain nodes (column 6, lines 39-41) of a mosfet transistor formed on the insulator substrate;

said continuous silicide layer further forming a sidewall butted connection structure used in conjunction with a gate interconnect layer;

wherein the continuous silicide layer consists of a first silicide film formed of silicon from the active region and a second silicide film formed of silicon from the gate interconnect layer.

Noda in view of Bryant does not expressly disclose the claimed inverter configuration, although the SRAM structure of Noda/Bryant could be used as a foundation for that structure. Sundaresan (e.g., Figs. 1, 3) discloses an SRAM cell similar to that of Noda/Bryant that includes inverter structures. It would have been obvious to one of ordinary skill in the art at the time of the invention to use the inverter structure of Sundaresan for the device of Noda/Bryant for the purpose, for example, of configuring a basic memory scheme known in the art, to provide low standby current (Sundaresan; column 1, lines 10-35).

In re claim 9, Noda in view of Bryant and further in view of Sundaresan discloses the device of claim 8, wherein the active region further connects to a source node of a least on pass gate (Sundaresan; column 3, lines 7-10).

In re claim 10, Noda in view of Bryant and further in view of Sundaresan discloses the device of claim 9, wherein the pass gate's drain node is connected to an access line.

In re claim 11, Noda in view of Bryant and further in view of Sundaresan discloses the device of claim 8, further comprising a first metal layer for forming wordline metal straps and landing pads for power supply lines and access lines.

In re claim 12, Noda in view of Bryant and further in view of Sundaresan discloses the device of claim 11, further comprising a second metal layer for forming power supply lines and access lines (column 6, lines 64-65).

In re claim 13, Noda in view of Bryant and further in view of Sundaresan discloses the device of claim 12, wherein the access lines are interposed between the power supply lines.

In re claim 14, Noda in view of Bryant and further in view of Sundaresan discloses the device of claim 11, wherein lines on the first and second metal layers are arranged in a substantially perpendicular position.

In re claim 16, Noda in view of Bryant and further in view of Sundaresan discloses the device of claim 15, further comprising a first metal layer (Sundaresan; column 4, lines 40-41) for forming landing pads for at least one wordline and at least one power supply line or access line.

In re claim 17, Noda in view of Bryant and further in view of Sundaresan discloses the device of claim 15, wherein the first metal layer is also used for forming a connection between the drain nodes of the two transistors of the first or second inverter.

In re claim 18, Noda in view of Bryant and further in view of Sundaresan discloses the device of claim 16, further comprising a second metal layer for forming at least one wordline metal strap and landing pads for at least one power supply line or access line (Sundaresan, column 6, lines 64-65).

In re claim 19, Noda in view of Bryant and further in view of Sundaresan discloses the device of claim 18, further comprising a third metal layer for forming power supply lines and access lines.

In re claim 20, Noda in view of Bryant and further in view of Sundaresan discloses the device of claim 19, wherein the access lines are interposed between the power supply lines (Sundaresan, column 6, lines 67-68 to column 7, lines 1-22).

In re claim 21, Noda in view of Bryant and further in view of Sundaresan discloses the device of claim 15, further comprising at least one active region with a silicide layer formed thereon serving as an intra-cell connection layer connecting drain nodes of the transistors of the first inverter.

In re claim 22, Noda in view of Bryant and further in view of Sundaresan discloses the device of claim 15, wherein the sidewall butted connection structure is electrically connected to a source node of a pass gate (Sundaresan; column 3, lines 7-10).

In re claim 23, Noda in view of Bryant and further in view of Sundaresan discloses the device of claim 15, further comprising a first metal layer for forming at least one power supply line and at least one access line.

In re claim 24, Noda in view of Bryant and further in view of Sundaresan discloses the device of claim 23, wherein the first metal layer is used for forming landing pads for at least one wordline, or landing pads for at least one power supply line.

In re claim 25, Noda in view of Bryant and further in view of Sundaresan discloses the device of claim 23, further comprising a second metal layer form forming

at least one wordline metal strap and at least one power supply line (Sundaresan, column 6, lines 64-65).

Response to Arguments

Applicant's arguments with respect to claims 1-25 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

The previous office action is withdrawn and this action is sent in its place.

Applicant's amendment of 11/01/05 necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jesse A. Fenty whose telephone number is 571-272-1729. The examiner can normally be reached on M-F 5/4.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ken Parker can be reached on 571-272-2298. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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